Appl. No. 10/665,809
Amdt. dated January 12, 2009
Amendment under 37 CFR 1.116 Expedited Procedure
Examining Group 2452

PATENT

REMARKS/ARGUMENTS

Claims 1-4, 6, 8-14 and 16-17 are pending in the application stand rejected.

Claims 6, 8-14 and 16 are rejected under 35 USC 112 as being indefinite.

Claims 12 and 16 are rejected under 35 USC 103 as being unpatentable over United States Patent 7,065, 072 to Quiles et al. (hereinafter "Quiles") in view of United States Patent Application Publication 2002/0103921 to Nair et al. (hereinafter "Nair").

Claims 1-3, 6, 8, 11, and 17 are rejected under 35 USC 103 as being unpatentable over Quiles in view of Nair and further in view of United States Patent 6,597,689 to Chui et al. (hereinafter "Chui").

Claims 6 and 11-14 are amended. No new matter has been added by the claim amendments.

As discussed below, Applicants respectfully submit that the cited references, whether taken alone or in combination, fail to disclose each and every element as set forth in the claims. In particular, primary reference Quiles does not disclose or fairly suggest first and second control processors configured to manage data routing paths for a first set of data processors and a second set of data processors, respectively. Also, none of the cited references discloses routing data *between* the data processors of a logical node as claimed. Accordingly, reconsideration and allowance of all claims is respectfully requested.

Rejections under Section 112

Claims 6 and 12 have been amended and it is believed that the issues identified in the Office Action have been addressed. Withdrawal of the rejections under 35 USC 112 is respectfully requested.

Rejections under Section 103

A. Claim 12

Claim 12 recites a method for routing packet data over a communication network using a telecommunications device that includes a plurality of data processors. The method

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includes "managing routing paths within the first logical node with a first control processor distinct from the first set of data processors; managing routing paths within the second logical node with a second control processor distinct from the second set of data processors." The method includes "routing the data associated with the first network service provider <u>between</u> <u>data processors of the first logical node</u> according to a first mapping of the first control processor... and routing the data associated with the second network service provider <u>between</u> <u>data processors of the second logical node</u> according to a second mapping of the second control processor." (emphasis added). Quiles in view of Nair does not disclose at least these elements as claimed.

The Office Action cites col. 4, lines 39-67 of Quiles as teaching the first and second control processors. <u>See</u>, Office Action at page 4. Specifically, Quiles' network interfaces 66, 68 are identified as teaching the claimed control processors. However, as disclosed in the reference, only one network interface card is used to communicate data at the digital subscriber line access multiplexer (DSLAM) 44 at a time. In particular, Figure 2 shows that only network interface card 66 is connected to the IP/ATM network 18. As disclosed by Quiles, network interface card 68 is simply a backup device and can be omitted. <u>See</u>, Quiles at col. 4, lines 56-58 ("Network interface card 68 may serve as a backup for network interface card 66. In some embodiments, network interface card 68 is omitted."

Accordingly, Quiles does not disclose the use of first and second control processors in connection with routing data received for first and second service providers. Much less, Quiles in no way suggests that a first control processor manages paths within a first logical node and a second control processor manages paths within a second logical node. Although Quiles does mention that *line cards* 87 are associated with different carriers, there is no disclosure whatsoever that *network interface cards* 66,68 manage routing paths for different groups of data processors (or line cards). Accordingly, Quiles does not disclose or suggest at least "<u>managing routing paths within the first logical node with a first control processor</u> distinct from the first set of data processors; <u>managing routing paths within the second logical node with</u> <u>a second control processor</u> distinct from the second set of data processors." (emphasis added).

Beyond these deficiencies, the combination of references fails to disclose "routing the data associated with the first network service provider between data processors of the first logical node according to a first mapping of the first control processor...and routing the data associated with the first network service provider between data processors of the second logical node according to a second mapping of the second control processor." (emphasis added).

The Office Action acknowledges that Quiles does not teach routing data between data processors as claimed, but maintains that these limitations are disclosed by Nair at paragraphs [0028]-[0032]. See, Office Action at page 4. Specifically, the Office Action argues that Nair's distributed service routers (DSR) route data within a carrier's line cards. Id.

However, Nair discloses that data traffic is "assigned to any one of the DSRs for routing, and to a corresponding one of the lines cards for forwarding." (emphasis added). See, Nair at [0028]. As disclosed in the reference, Nair's "routing system" includes one DSR and a corresponding one of the line cards. There is no teaching or suggestion that a DSR routes data between line cards, nor is there is any disclosure of routing paths within a logical node. Accordingly, Applicants respectfully submit that the cited references fail to disclose each and every element as set forth in claim 12.

Finally, Applicants respectfully submit that a person of skill in the art would not be motivated to combine references and that the Office Action has not identified any reason for doing so. The Office Action simply indicates motivation would be "so that customers can communicate with each other." See, Office Action at page 5. However, customers can communicate with each other without modifying either reference. It is therefore respectfully submitted that there would be no reason to modify either reference for this purpose.

B. Claims 1, 6

Claims 1 and 6 each recite limitations similar to those discussed in connection with claim 12 and each claim is rejected using a similar rationale. Tertiary reference Chui is cited as teaching routing data according to a physical location of line cards. See, Office Action at page 7. However, Applicants respectfully submit that Chui does not cure the deficiencies of

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Quiles/Nair as previously discussed and that the extended combination of references fails to teach or suggest each and every element as claimed.

With regard to claim 1, the combined references also fail to disclose a plurality of logical nodes "associated with a control processor in the plurality of control processors such that each control processor is coupled to a first data processor of its associated logical node and manages data routing paths for the logical node in relation to said first data processor." None of the cited references discloses or even suggests that a control processor manages routing paths *in relation to* a first data processor in a logical node.

In the passage from Chiu that is cited in the claim rejection, Chiu simply indicates that VPI/VCI numbers are linked to port numbers. See, Chui at col. 26, lines 35-37. There is no teaching or suggestion that a control processor manages routing paths *in relation to a first data processor* of a logical node. To the contrary, Figure 5 of Chui shows that data traveling from the telecommunications backbone passes *from one switch to one line card* on its way to the DSL side of the network. Thus, the combination of Quiles, Nair, and Chui does not teach or suggest data routing paths *between* data processors, much less that such data routing paths are managed in relation to a first data processor of a logical node.

With regard to claim 6, the cited references also fail to disclose "a first control processor separate from the first set of data processors configured to manage data routing paths between data processors of the first set according to their corresponding positions in the first logical shelf" or "a second control processor separate from the second set of data processors configured to manage data routing paths between data processors of the second set according to their corresponding positions in the second logical shelf" as claimed. Accordingly, Applicants respectfully submit that claims 1 and 6 are allowable over the cited reference for the reasons discussed in connection with claim 12 and also because they fails to teach or fairly suggest the limitations identified above.

C. Claims 2-4; 8-11; 13-14, 16-17

Claims 2-4 depend from claim 1. Claims 8-11 depend from claim 6. Claims 13-14 and 16-17 depend from claim 12. Each dependent claim incorporates all of the limitations of

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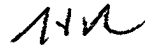Examining Group 2452

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its respective base claim. Accordingly, each dependent claim is believed to be patentable over the cited reference for at least the reason that it depends from an allowable base claim as well as being patentable for its further limitations. Reconsideration and allowance of all claims is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 858-350-6100.

Respectfully submitted,

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